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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Amit Gulati, Subramania I. Sudharsanan, Parthasarathy Sriram		
Assignee:	Sun Microsystems, Inc.		
Title:	Apparatus and Method for Scalable Buffering in a Digital Video Decoder		
Serial No.:	09/517,804	Filing Date:	March 2, 2000
Examiner:	Allen C. Wong	Group Art Unit:	2183
Docket No.:	P3480	Customer No.:	33438

Austin, Texas
February 22, 2005

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APPEAL BRIEF UNDER 37 CFR § 1.191

Dear Sir:

Applicants submit this Appeal Brief pursuant to the Notice of Appeal filed in this case on November 22, 2004.

Enclosed is a check in the amount of $620.00 to cover the $500.00 fee for the Appeal Brief and the $120.00 one month extension fee. The Commissioner is hereby authorized to deduct any additional amounts required for this appeal brief and to credit any amounts overpaid to Deposit Account No. 502264.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Sun Microsystems, Inc. as named in the caption above.

II. RELATED APPEALS

Based on information and belief, there are no appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-9, 12, 14 and 16-22 are pending in the application. Claims 1-9, 12, 14 and 16-22 have been rejected. Claims 1-9, 12, 14 and 16-22 are appealed. Appendix "A" contains the full set of pending claims.

IV. STATUS OF AMENDMENTS

No Amendments have been filed subsequent to final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention, as set forth by independent claim 1, relates to a method of assigning a buffer size in a video decoder (see, e.g., page 6, lines 26 – 30) which includes establishing a first buffer size for a scalable buffer (see, e.g., page 9, lines 21 – 24 and page 12, lines 20 – 21), processing a video data stream with the scalable buffer configured to the first buffer size (see, e.g., page 12, lines 26 – 28), selecting a second buffer size for the scalable buffer, processing the video data stream with the scalable buffer configured to the second buffer size, creating memory utilization data characterizing cache memory performance during the processing with the scalable buffer configured to the first buffer size and the processing with the scalable buffer configured to the second buffer size (see, e.g., page 13, lines 28 – 30), and assigning a buffer size that is dependent upon the first buffer size and the second buffer size for the scalable buffer in accordance with the memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer (see, e.g., page 12, lines 14 – 19).

The present invention, as set forth by independent claim 13, relates to a computer readable memory to direct a computer to function in a specified manner which includes a buffer management module(see, e.g., page 6, lines 5 – 10 and Figure 1, item 140) to establish a first buffer size and a second buffer size for a scalable buffer, a video decoding module to process a video stream with the scalable buffer configured to the first buffer size and then the second

buffer size, and an analysis module to create memory utilization data characterizing cache memory performance during the processing with the scalable buffer configured to the first buffer size (see, e.g., page 12, lines 26 – 28) and during the processing with the scalable buffer configured to the second buffer size(see, e.g., page 13, lines 28 – 30), the analysis module including a buffer size adjuster to assign a buffer size that is dependent upon the first buffer size and the second buffer size for the scalable buffer in accordance with the memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer (see, e.g., page 12, lines 14 – 19).

VI. GROUNDS FOR REJECTION

Caims 1 – 9, 13, 14 and 16 – 22 stand rejected over Cheney, U.S. Patent No. 5,668,599 (Cheney) in view of Smith, U.S. Patent No. 5,802,600 (Smith).

VII. ARGUMENT

Claims 1 – 9, 13, 14 and 16 – 22 are allowable over Cheney, U.S. Patent No. 5,668,599 (Cheney) in view of Smith, U.S. Patent No. 5,802,600 (Smith).

Cheney relates to a system that manages the performance of a main memory, through the use of a spill buffer in the main memory. While the spill buffer size may change, it varies only in accordance with parameters such as the operation modes and the frame sizes (see e.g., Figs. 12 – 15) and there is no relationship or dependency between one and another spill buffer size. I.e., given a set of video decoding and displaying parameters, the spill buffer size is completely determined.

Because Cheney does not teach a method of determining an optimal buffer size for a scalable buffer in accordance with the cache performance associated with a first and second buffer sizes, the spill buffer in Cheney is not equivalent to the scalable buffer as claimed in the present invention.

When discussing Cheney, the examiner sets forth that

> Cheney's fig.4, element 402 is an instruction storage that can similarly function like a cache where element 402 processes video data stream instructions and interactively functions with other elements of fig.4 such as decode subsystem 301, controller 401, etc. Thus Cheney discloses the *cache memory* 402 *is distinct* from the scalable buffer 601. (Final office action, page 2, emphasis in original.)

To support the position that Cheney teaches the determination of optimal buffer size and a scalable buffer, the Examiner sets forth:

> In col. 12, lines 13-45, fig.4, element 401 is the controller module or analysis module that is interactive with all parameters presented to element 401 for analysis. Cheney teaches the adjustment of a buffer size register and a spill size register for minimizing memory use and permit efficient decoding, and that since the elements function interactively together, there is a relationship between the buffers, as disclosed col.14, lines 25-36. In fig.4, Cheney's element 600 is a buffer management module that appropriates the first and second buffer sizes for scalable buffer 601 so as to appropriately store data with the right amount of space required for efficient memory management. Thus, Cheney teaches the determination of the optimal buffer size and the scalable buffer. (Final office action, pages 2,3.)

The section of Cheney to which the examiner refers sets forth:

> The Spill Buffer is used to accomplish this task [i.e., enabling successive B frames to reuse a portion of the same area in memory]. The Spill Buffer is an overflow buffer that is dynamically assigned to one of the three buffers.
>
> Hardware makes use of a buffer size register and a spill size register to create a logical buffer equal to the sum of each. Hardware automatically detects whether a buffer's logical address exceeds the buffer size and steers the address to point at the Spill Buffer. A combination of hardware and microcode manage the wrapping of logical addresses from the end of the Spill Buffer into the beginning of the frame buffer. (Cheney, Col. 14, lines 25 – 35, description of "this task" added.)

The cited section of Cheney does not disclose or suggest assigning a buffer size that is dependent upon the first buffer size and the second buffer size for the scalable buffer in accordance with the memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer, as required by the claims.

Smith teaches a method of dynamically adjusting the sizes of first and second portions of a cache memory in a data processing system where the first portion is allocated to storage of data blocks and the second portion is allocated to storage of directory entries so as to minimize the

sum of the expected cache miss rate and false invalidation rte. (See e.g., Smith, Col 3, line 51 – Col. 4, line 12.)

To support the position that Smith teaches determining an optimum buffer size for a scalable buffer in the main memory based upon the corresponding cache memory performance, the examiner sets forth:

> Also, Smith is relevant to the discussion to this case because it discloses the improving the allocation of memory and cache to minimize false cache reads and inaccurate storage and retrieval of data, as stated in col.3. lines 41-48. Smith is cited because Cheney fails to disclose the limitation of wherein the memory utilization data that includes cache miss rate data. Therefore, it would have been obvious to one of ordinary skill in the art to take the teachings of Cheney and Smith, as a whole, for utilizing the memory utilization data that includes the cache miss rate data so as to enhance, improve the cache memory performance. Doing so would speed the task of decoding high quality images for viewing and save costs in the long run with smooth, efficient memory performance routines. (Final office action, page 3.)

The section of Smith to which the examiner refers sets forth:

> Accordingly, it is an object of this invention to provide an improved system and method for controlling allocation of cache memory space as between directory entries and data blocks.
>
> It is another object of this invention to provide an improved system and method for controlling allocation of cache memory space which minimizes both false invalidations and cache read misses. (Smith, Col. 3, lines 41 – 48.)

The cited section of Smith, and nowhere within Smith is there discussion of assigning a buffer size that is dependent upon the first buffer size and the second buffer size for the scalable buffer in accordance with the memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer. Accordingly, Smith also does not disclose or suggest assigning a buffer size that is dependent upon the first buffer size and the second buffer size for the scalable buffer in accordance with the memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer, as required by the claims.

More specifically, Cheney and Smith, taken alone or in combination, do not teach or suggest a method of assigning a buffer size in a video decoder which includes establishing a first

buffer size for a scalable buffer, processing a video data stream with said scalable buffer configured to said first buffer size, selecting a second buffer size for said scalable buffer, processing said video data stream with said scalable buffer configured to said second buffer size, creating memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and the processing with said scalable buffer configured to said second buffer size, and assigning a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer, all as required by claim 1. Accordingly, claim 1 is allowable over Cheney and Smith. Claims 2 – 9 depend from claim 1 and are allowable for at least this reason.

Cheney and Smith, taken alone or in combination, do not teach or suggest a computer readable memory to direct a computer to function in a specified manner which includes a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer, a video decoding module to process a video stream with said scalable buffer configured to said first buffer size and then said second buffer size, and an analysis module to create memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and during the processing with said scalable buffer configured to said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer., all as required by claim 13. Accordingly, claim 13 is allowable over Cheney and Smith. Claims 14, and 16 – 22 depend from claim 13 and are allowable for at least this reason.

IX. CONCLUSION

For the above reasons, Applicants respectfully submit that rejection of pending claims 1 – 9, 13, 14 and 16 – 22 is unfounded. Accordingly, Applicants request that the rejection of claims 1 – 9, 13, 14 and 16 – 22 be reversed.

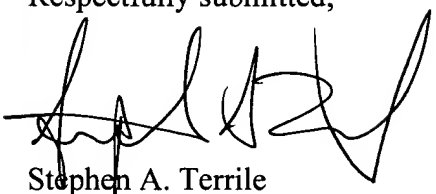
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 22, 2005.

Attorney for Applicant

2/22/05

Date of Signature

Respectfully submitted,



Stephen A. Terrile
Attorney for Applicant
Reg. No. 32,946

APPENDIX "A"

1. A method of assigning a buffer size in a video decoder, comprising:

establishing a first buffer size for a scalable buffer;

processing a video data stream with said scalable buffer configured to said first buffer size;

selecting a second buffer size for said scalable buffer;

processing said video data stream with said scalable buffer configured to said second buffer size;

creating memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and the processing with said scalable buffer configured to said second buffer size; and

assigning a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data;

wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer.

2. The method of claim 1 wherein said establishing and said selecting each include defining a buffer size as a multiple of a buffer size for storing a single macroblock.

3. The method of claim 1 wherein said processing includes utilizing said scalable buffer with a variable length decoder.

4. The method of claim 1 wherein said processing includes utilizing said scalable buffer with an inverse discrete cosine transfer function module.

5. The method of claim 1 wherein said processing includes utilizing said scalable buffer with a motion compensator.

6. The method of claim 1 wherein said creating includes creating cache utilization data defining data cache miss rates.

7. The method of claim 1 wherein said creating includes creating cache utilization data defining instruction cache miss rates.

8. The method of claim 1 further comprising modifying the size of video data stream processing instructions to correspond to said buffer size selected in said assigning step.

9. The method of claim 8 wherein said modifying includes loop unrolling vide data stream processing instructions to correspond to said buffer size selected in said assigning step.

13. A computer readable memory to direct a computer to function in a specified manner, comprising:

a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer;

a video decoding module to process a video stream with said scalable buffer configured to said first buffer size and then said second buffer size; and

an analysis module to create memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and during the processing with said scalable buffer configured to said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data;

wherein the memory utilization data includes cache miss rate data and the cache memory is distinct from the scalable buffer.

14. The computer readable memory of claim 13 wherein said buffer management module establishes said first buffer size as a first multiple of a buffer size for storing a single macroblock and said second buffer size as a second multiple of a buffer size for storing a single macroblock.

16. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a variable length decoder.

17. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with an inverse discrete cosine transfer function module.

18. The computer readable memory of claim 13 wherein said video decoding module utilizes said scalable buffer with a motion compensator.

19. The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining data cache miss rates.

20. The computer readable memory of claim 13 wherein said analysis module creates cache utilization data defining instruction cache miss rates.

21. The computer readable memory of claim 13 wherein said analysis module further includes a subsystem to modify the size of video data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.

22. The computer readable memory of claim 21 wherein said subsystem performs loop unrolling of video data stream processing instructions to correspond to said buffer size assigned by the buffer size adjuster.